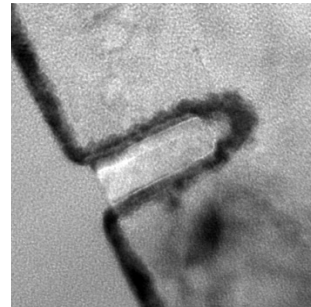
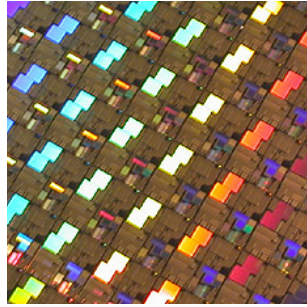
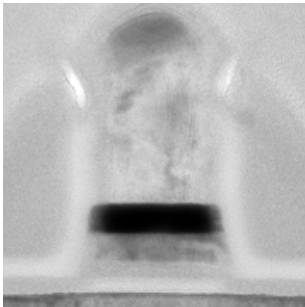


## Materials Drive the Future



SEMATECH's Front End Processes and  
Emerging Technologies Program



# SEMATECH: The world's catalyst for accelerating the commercialization of technology innovations into manufacturing solutions.

The next technology revolution won't come from a lab. It won't be driven by a single company. It will come from effective collaboration and smart partnerships that translate today's innovative ideas into the products of tomorrow.

At SEMATECH the world comes together to speed the commercialization of technology innovation, from research and development to manufacturing.



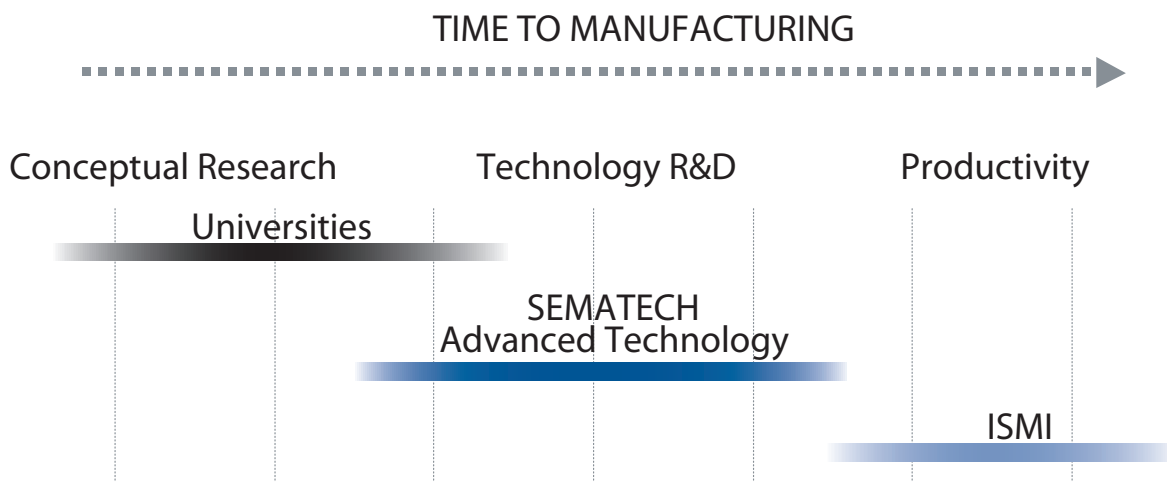
## Lithography, Interconnect, Materials and Emerging Technology

SEMATECH conducts state-of-the-art research on the technical challenges and costs associated with developing new materials, processes, and equipment for semiconductor manufacturing. Advanced technology programs focus on immersion and EUV lithography, low-k materials and 3D architecture, and high-k materials and next generation transistors.

## Manufacturing Productivity

International SEMATECH Manufacturing Initiative (ISMI) operates six programs encompassing a total of 30 projects—all focused on increasing productivity and decreasing costs for our members. They include:

- ESH Technology Center
- Continuous Improvement
- ISMI Councils
- Metrology
- Next Generation Factory
- 450 mm Transition



## At SEMATECH, some of the biggest names in the semiconductor business come together to leverage resources, increase productivity, and lower costs.

We have a proven history of making sure member companies can afford to stay on the productivity curve.

### We reduce cost and risk

We are a companion to members' R&D processes and help develop aspects of technology more quickly and economically than members could on their own by reducing options to the most workable solutions.

Rather than each member company funding solutions individually, we enable members, using what they learn at SEMATECH, to spend more resources on developing their own competitive advantage.

### We deliver exclusive benefits to our members

First-to-market solutions – Members get full and detailed, actionable data.

Cost avoidance – Members avoid spending the full R&D costs of ultimately unworkable solutions and lower their learning curve for new processes.

Inside track – Members receive early evaluation of new materials and technologies without contamination and equipment risk in their fabs.

### We are flexible both in memberships and programs

Members help shape the programs.

We offer a variety of ways to work with us.

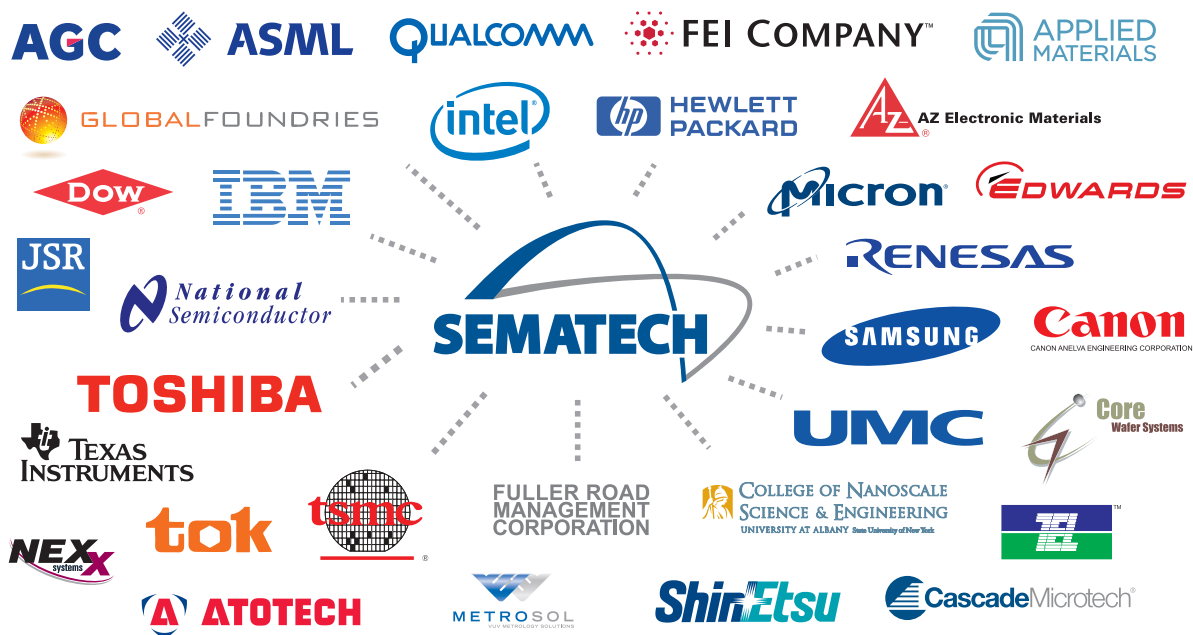
We span the timeline from research to development to manufacturing.

### We have a proven record of success

We have nearly 20 years of experience in moving the industry forward.

SEMATECH is a well-cited and long-standing example of a successful public/private partnership.

During a period of rising industry uncertainty, it becomes increasingly important to spend R&D money wisely. SEMATECH believes that building strategic collaborations to avoid unnecessary costs while staying close to emerging innovations is the best way to keep your company moving forward as the industry creates the next technology revolution.



## Front End Processes and Emerging Technologies Program

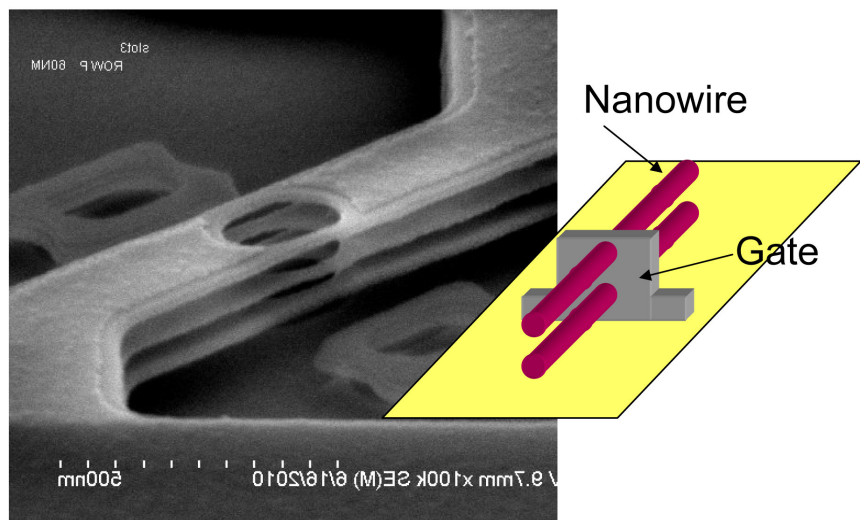
SEMATECH's Front End Process (FEP) program focuses on screening, developing, and characterizing cutting-edge new materials, processes, tools, characterization and reliability methodologies, as well as device models and designs, that enable scaling CMOS logic, memory, and emerging technologies beyond CMOS. These technologies in the front end of a process flow are the heart of transistor and memory device fabrication technologies for chip-makers and the core activities of SEMATECH's FEP group.

We have a number of key R&D projects, including aggressively scaled (to 0.5 nm) high-k gate dielectrics on Si, appropriate metal gates (electrodes) for threshold voltage control in low standby power (LSTP) and high performance applications, high mobility channels using Ge-based and III-V based materials, non-planar transistor structures, advanced non-volatile memory devices and associated materials, and characterization and device models.

All these advanced materials and process technologies must be realized while meeting the specifications for capacitance equivalent thickness, threshold voltage ( $V_t$ ), mobility, reliability, and many other parameters. FEP is actively working on alternative materials to Si channels, such as Si(Ge) and III-V, that are applicable for the 16 nm node and beyond. A significant part of this effort is focused on developing low defect density epitaxial Ge/III-V layers on Si and suitable techniques to form high quality high-k gate stacks, low contact resistance silicides, ultra shallow junctions, etc. Also being investigated is non-planar device development centered on high mobility FinFETs and nanowire FETS, which can provide better electrostatic control

and scalability than current planar device architectures. Novel materials to address the aggressive scaling of flash memory technologies, as well as emerging memories like resistive RAMs, are likewise being explored.

SEMATECH's FEP program is also extensively involved in developing novel electrical/physical characterization methods to reveal the fundamental nature of the various materials used in device fabrication and the interactions between them. In collaboration with its member companies, the SRC, leading universities, and national labs, our group ensures that the needed methods and models are developed and drives for common benchmarking standards to accelerate learning and commercial adoption. Working with member companies, equipment and materials suppliers, and other partners, the FEP team also develops the needed infrastructure in materials, processes, and tools to enable the adoption of future effective scaling options, often shaping the direction of the ITRS.



Beyond planar CMOS and FinFETs will be nanowires. Shown above is a 3-layer stack of nanowires (prior to gate formation).

## Programs

- Advanced Dielectrics and Electrodes
  - » High-k dielectrics for gate stacks and memories
  - » Metal electrodes for gate stacks and memories
  - » Disruptive and emerging memory technologies
- Advanced CMOS Scaling
  - » High mobility Ge and III-V channels and devices
  - » Ultra-shallow junctions and low R contacts for Si and high mobility channels
  - » Non-planar CMOS: FinFETs, nanowires, including Si and high mobility channels
- Electrical & Physical Characterization
  - » Novel characterization methodology development
  - » Reliability methodology development and assessment
  - » Physical characterization of materials and interfaces
- Emerging Technologies
  - » Ultra-low power devices and materials
  - » Design/variability aware technologies
  - » NEMS and sensors
  - » Energy technologies

## Research and Development

Our core technical teams are consistently producing the most innovative techniques for extending high-k dielectrics, metal gates, junction and silicide contact technologies, and advanced memory technologies, while making breakthroughs in developing solutions with new high mobility channel materials and devices, FinFETs and nanowire devices, emerging memory devices, and technologies beyond CMOS devices in the “More than Moore” space.

These efforts aim not only to extend incumbent technologies but also to enable future low and ultra-low power devices, which are increasingly important for mobile as well as cloud computing systems. As these path-breaking solutions are developed, the focus remains on providing a strong foundation in understanding the fundamental material properties, process options, integration choices, reliability impacts, costs, and complexity trade-offs that drive the scaling of device technology and its adoption into high volume manufacturing.

In the arena beyond CMOS, teams have focused on developing ultra-low to no leakage devices, multifunctional high temperature stable devices and sensors, and analog/mixed signal components that can be deployed in conjunction with CMOS devices on the same Si platform to enhance functionality. Such heterointegration options are critical for the future system-on-chip (SoC) designs that are on the roadmaps of many leading chip makers.

SEMATECH continues to expand its R&D portfolio of emerging materials and devices beyond CMOS that promise to revolutionize information technologies.

# Front End Processes and Emerging Technologies Program

## Technical Milestones

**2004** – Engineers developed stable high-k gate stacks in the equivalent oxide thickness (EOT) range of 0.6–1.0 nm as well as the much cited (and used) terraced oxide structure to accurately extract the effective work function of metal gates.

**2005** – A team of engineers identified a handful of materials that can be used to build dual work function metal gate electrodes. The result is a gate stack with metal electrodes that exhibit significantly different work functions, mimicking a critical electrical polarity of conventional poly-silicon gates.

**2006** – Good progress was recorded on higher-k materials for future gate stack scaling, ultra-shallow junctions down to 9 nm, and high mobility (1.5–2.5X of Si hole mobility) selective SiGe and Ge epitaxial layers.

**2007** – Technologists demonstrated dual metal gates for high-k CMOS devices that will enable the 45 nm and 32 nm technology generations. A comprehensive understanding of and opportunities to control  $V_{fb}/V_t$  roll-off, especially for scaled high-k metal gate pFETs, were demonstrated.

**2008** – Sophisticated characterization of highly scaled dielectric films led to the fundamental understanding that helped to scale the electrical thickness of dielectrics (EOT <0.6 nm) while retaining performance for future generation devices. Scaled FinFETs were demonstrated with Si and high mobility SiGe channels.

**2009** – Breakthroughs in reducing the Schottky barrier height in contacts and new ultrashallow junction ( $X_j \sim 5$  nm or better) formation techniques with little or no damage were demonstrated, paving the way to meet the needs of the 22 nm generation nodes. Good progress was also recorded in Ge and III-V device modules (gate stack CET  $\sim 1$  nm, damage-free junction formation, 3-5X Si mobility), and emerging RRAM memory development.

## Recent Advancements

Recently, SEMATECH's FEP engineers demonstrated for the first time that hafnium-oxide films with a zero low-k silicon-oxide interface scale better than exotic higher-k materials, providing a practical, scalable option for manufacturers. Additionally, FEP delivered a systematic study explaining low drive currents in germanium-based n-channel metal-oxide semiconductor FETs (MOSFETs).

Other advancements include the following:

- Demonstrated significant reductions in Schottky barrier height and contact resistance, enabling the continued enhancement of device performance beyond the 45 nm technology node. Contact resistance in source/drain regions, which comes from a relatively high Schottky barrier between n-type doped Si and nickel silicide, is one of the most pressing concerns in advanced CMOS technology.
- FEP demonstrated novel doping and activation schemes to form defect-free ultra shallow junctions with a low resistivity for Si and non-Si channels in planar and non-planar forms.
- For the first time ever, SEMATECH demonstrated highly scaled FinFETs with high mobility SiGe channels exhibiting excellent electrostatics and transport for continued scaling in non-planar architectures.
- SEMATECH demonstrated the feasibility to fully integrate III-V on Si on 200 mm wafers and form highly scaled devices using standard fab Si processing tool sets. This is a significant achievement in terms of developing the infrastructure for III-V VLSI processing in a Si line.
- SEMATECH demonstrated the first Si-based tFET with low subthreshold swing (SS) ( $\sim 42$  mV/dec) and reasonable Ion ( $\sim 50$  micro-amp/micron).

- FEP developed and demonstrated of an in-line metrology system based on vacuum ultraviolet spectroscopic reflectometry (VUV-SR) for characterizing ultra-thin layers in gate dielectric stacks and thin SiGe layers for substrate engineering. This platform will be able to provide the highly accurate characterization needed for the in-line metrology of advanced logic and memory applications for future technology generations.
- Conventional characterization techniques that work with Si substrates do not necessarily work with III-V substrates, as is the case with characterizing the interface between the III-V substrate and dielectric. For this, a new physical technique has been developed, second harmonic generation (SHG), which has been shown to correlate nicely with electrical results.
- A key new mask set has been developed with test structures not only focused upon a range of devices (FinFETs, nanowires, and resistive RAM, in addition to conventional planar devices), but those intentionally designed to allow a connection from design to integration to test and reliability.
- As new materials are introduced, the long-term behavior of devices, reliability in particular, are of concern. To address this, the group, along with software specialists, has developed a foundation for both testing and analyzing reliability data for a range of devices.
- Low frequency noise (LFN) is a rising issue for circuits, as the signal-to-noise ratio limits continue to be tested as devices are scaled. The testing capability for both LFN and the related random telegraph signal has been established in our newest lab; results have led to a model (including the energy of physical relaxation of the bonds around a trap) that appears to explain several issues that earlier noise models could not address.
- For memory devices, we have focused upon resistive RAM devices, concentrating on material sets that can be easily incorporated into manufacturing sites. Although more exotic materials have shown promise in the literature, we have found that with creative integration techniques excellent switching characteristics are possible with conventional materials.

## Future Goals

Recognizing that disruptive technology has become the norm for the industry to keep pace with Moore's Law, FEP has adopted an ambitious strategy for the next five years. Major goals include the following.

- Low standby power/low operating power: FEP acknowledges the industry drive to deliver high performance at low power and to deliver solutions through a combination of the careful analysis of key parasitic components and intelligent introduction of new materials.
- Low power: SEMATECH FEP is constantly evaluating novel device schemes by changing device design, enabling devices that can work at  $<0.5V$ . This is done by beating the 60 mV/dec (KT/q) sub-threshold slope and provide ultra low leakage/power (low  $I_{off}$  and  $V_{cc}$ ) devices with good performance. The goal is to compare and contrast (based on experiments and simulation) the opportunities with tunneling-based FETs, NEMs, negative capacitance FETs, etc.
- Disruptive scaling for silicon: FEP is making a significant leap in effective dielectric thickness by moving away from conventional clean/deposition in an effort to eliminate the SiO<sub>x</sub> interfacial layer underneath the high-k.
- Disruptive technology for fins, and nanowires, and III-V substrates: We are looking beyond planar Si MOSFETs to continue scaling; develop production-quality non-planar structures (FinFETs and nanowires) that provide significant enough advantages over planar Si to justify the changes required; and develop planar III-V-on-Si-substrates that enable running these promising new material sets through conventional Si fabs with minimal contamination concerns to facilitate their introduction in the 11 nm node or beyond.
- Disruptive scaling for memory technologies using resistive RAM (ReRAM): FEP has enable well-controlled ReRAM memory cells for adoption by member companies by integrating the memory with a transistor for compliance control and assuring that the material systems for the ReRAM are easily fab-compatible.

## Recent Publications

Gate Diode investigation of Bias Temperature Instability in High-k FinFETs

Author: Chadwin Young

Publication: *IEEE Electron Device Letters* (Apr 2010)

Pulsed Id-Vg methodology and its application to the electron trapping characterization of high-k gate dielectrics

Author: Chadwin Young

Publication: *Journal of Semiconductor Technology and Science* (Apr 2010)

Analyzing electron trap properties in gate stack of modern MOSFETs

Author: Dmitry Veksler

Publication: *IEEE TDMR* (Apr 2010)

Hot carrier injection from angstrom-scale SOI films measured by optical second-harmonic generation

Author: Jimmy Price

Publication: *APL* (Apr 2010)

Analyzing electro trap properties in gate stack of modern MOSFETs

Author/s: Dmitry Veksler

Publication: *IEEE TDMR* (Mar 2010)

Substrate Hybridization and Rippling of Graphene Evidenced by Near- Edge X-Ray Absorption Fine Structure Spectroscopy

Author: Pat Lysaght

Publication: *Journal of Physical Chemistry Letters* (Feb 2010)

Enter Reducing Rext in Laser Annealed Enhancement-Mode In<sub>0.53</sub>Ga<sub>0.47</sub>As Surface Channel n-MOSFET

Author: Injo Ok et al.

Publication: *VLSI-TSA* (June 2010)

Degradation of tunnel oxide in TANOS devices and its origin

Author: Hokyung Park et al.

Publication: *VLSI-TSA* (June 2010)

Improved Interface Characterization Technique for High-k/Metal Gated MugFETs Utilizing a Gated Diode Structure

Author: Chadwin Young

Publication: *VLSI-TSA* (June 2010)

Alternative Approaches for High-k /Metal Gate CMOS: Low Temperature Process (Gate Last) and SiGe Channel

Author: C.S. Park et al.

Publication: *VLSI-TSA* (June 2010)

Synchrotron XPS and EXAFS Identification of Chemical State and Crystal Phase Changes of HfO<sub>2</sub> Films Doped with Si, N, Al, and La

Author: Pat Lysaght et al.

Publication: *VLSI-TSA* (June 2010)

Characterization of sub-nm AlO<sub>x</sub> and LaO<sub>x</sub> capping layers on high-k gate stack film systems using VuV ( $\lambda=120\text{nm}$ ) reflectivity

Author: Jimmy Price et al.

Publication: *VLSI-TSA* (June 2010)

Strain Engineering in Nanoscale CMOS FinFETs and Methods to Optimize RS/D

Author: Casey Smith et al.

Publication: *VLSI-TSA* (June 2010)

Enhanced Performance in SOI FinFETs with Low Series Resistance by Aluminum Implant as a Solution Beyond 22nm Node

Author: Injo Ok et al.

Publication: *VLSI-TSA* (June 2010)

SiGe CMOS on (110) Channel Orientation with Mobility Boosters: Surface Orientation, Channel Directions, and Uniaxial Strain

Author: Jungwoo Oh et al.

Publication: *VLSI-TSA* (June 2010)



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